REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-20 are pending in this application. Claims 12-20 are added by the present response. No new matter is believed to be added. Claims 1-11 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 7,020,854 to Killian et al. (herein "Killian"). That rejection is traversed by the present response as discussed next.

Each of independent claims 1 and 6 is amended by the present response to clarify features recited therein, and to particularly clarify "selecting at least one of a plurality of option instructions that are provided respectively in correspondence with machine instructions to be implemented within said processor and described in general-purpose language". New claims 12-15 are dependent claims dependent on amended independent claims 1 and 6. New claim 16 is an independent claim directed to a method for designing a processor core used in a processor with a memory operatively coupled to the processor core. Those method claims recite features from independent claim 1. New claims 17-20 are dependent claims that depend on new independent claim 16.

The claims as written are directed to allowing efficient design in the field of semiconductor intellectual property. In respect to semiconductor intellectual property, being able to efficiently reuse existing designs can provide an important advantage, particularly as many semiconductor intellectual properties have been designed in HDL such as VHDL and Verilog.

One feature realized by the claimed inventions is to utilize user defined instructions in general-purpose language for designing a processor core. Such a structure makes it possible to reuse existing HDL resources. Particularly, user defined instructions are typically described in two languages, RTL description and behavior level description or C/C++ model description. The use of a RTL description enables optimized RTL description after high level

synthesis. The use of behavior level description or C/C++ model description enables rapid regeneration of a software environment.

With the claimed inventions the user defined instruction in general-purpose language enhances reusing existing HDL resources in a semiconductor design environment.

The features recited in the claims are believed to clearly distinguish over the applied art to Killian.

The outstanding rejection cites Killian to disclose "selecting at least one of a plurality of option instructions that are provided respectively in correspondence with machine instructions to be implemented within said processor core" at column 24, lines 56-60, column 6, lines 65-67, and column 29, lines 50-54.

The claims as written are believed to clearly distinguish over the noted disclosures in Killian. More specifically, in Killian all the user defined instructions have the same format and operand usage in accordance with Tensilica Instruction Set Extensions (TIE) codes (see for example Killian at column 16, lines 23-40).

In contrast to Killian, in accordance with the claimed invention the user defined instructions are described in general-purpose language. As non-limiting examples, that general-purpose language can be a RTL description and behavior level description or C/C++ model description, which features are recited in certain of the dependent claims. Killian does not disclose or suggest such features.

Further, in Killian the TIE language allows a user to describe custom functions for applications in the form of extensions and new instructions to augment a base instruction set architecture (ISA). Given the TIE specification of the designer-defined opcodes and their corresponding operands, Killian discloses generating a C header file is a straightforward process of translating to the GNU C complier inline assembly syntax (see for example Killian at column 26, line 22 et seq.).

In Killian the use of TIE permits rapid specification of new instructions. A configuration processor generator can fully implement the instructions in both a hardware implementation and software development tools that support new instructions in C and C++ compilers, an instruction set simulator, and so forth. Because of the rapid regeneration of hardware and software in Killian the TIE language would appear to provide easy handling and to be user friendly.

However, as discussed above, such a system as in Killian has a drawback in not being able to efficiently reuse existing designs for semiconductor intellectual property, for example that have been designed in HDL such as VHDL and Verilog.

The present invention allows to reuse existing HDL resources because user defined instructions are described in a general-purpose language, and Killian does not disclose or suggest such a feature. Killian does not disclose or suggest such features.

Thereby, each of amended independent claims 1 and 6, and new independent claim 16, and the claims dependent therefrom, are believed to clearly distinguish over Killian.

With respect to independent claim 10, independent claim 10 recites "preparing a configuration specifying a file including variable item definition information concerning a multiprocessor configuration". With respect to that limitation the outstanding rejection cites Killian at column 45, lines 28-30. Applicants note that disclosure in Killian is merely the preamble of claim 1 in Killian that does not address any specifying of a file, particularly including variable item definition information concerning a multiprocessor configuration. That broad preamble statement in Killian being directed to a method designing a configurable pipeline processor does not correspond to that claim feature.

Moreover, Killian further does not disclose or suggest the variable item definition information including "at least one item of option instruction information and information concerning a user defined module and a multiprocessor configuration". With respect to that

feature the outstanding rejection also refers to Killian at column 45, lines 28-30, which again is merely the preamble of claim 1 in Killian that does not provide any disclosure as claimed.

In such ways independent claim 10, and claim 11 dependent therefrom, are also believed to distinguish over Killian.

In view of the present response applicants respectfully submit the claims as written distinguish over Killian.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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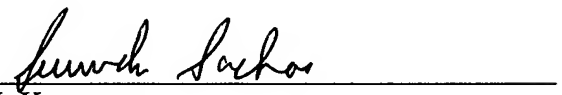

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